

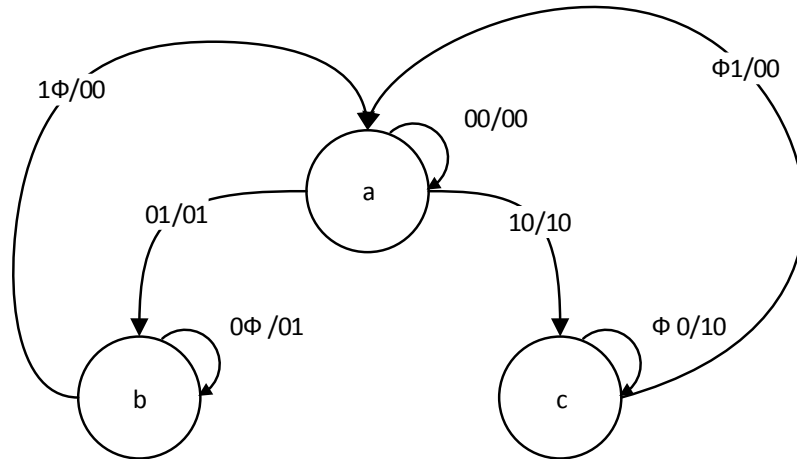
Examen Primer Parcial

Digitales II

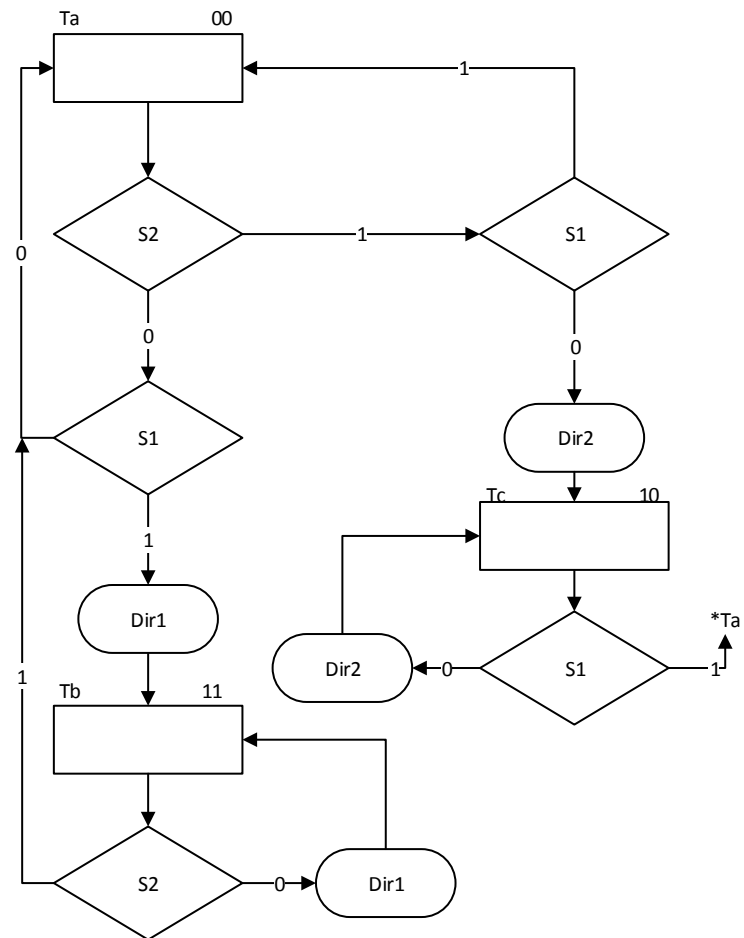
II Término 2014-2015

Problema # 1

1a)



1b)



1c)

Y1					Y0				
y_1y_0/s_2s_1	00	01	11	10	y_1y_0/s_2s_1	00	01	11	10
00	0	Φ	1	1	00	0	Φ	0	1
01	1	Φ	1	0	01	1	Φ	0	0
11	Φ	Φ	0	0	11	Φ	Φ	0	0
10	1	Φ	0	1	10	0	Φ	0	1

Dir2					Dir1				
y_1y_0/s_2s_1	00	01	11	10	y_1y_0/s_2s_1	00	01	11	10
00	0	0	0	1	00	0	0	1	0
01	0	0	0	0	01	1	0	1	0
11	0	0	0	0	11	0	0	0	0
10	1	0	0	1	10	0	0	0	0

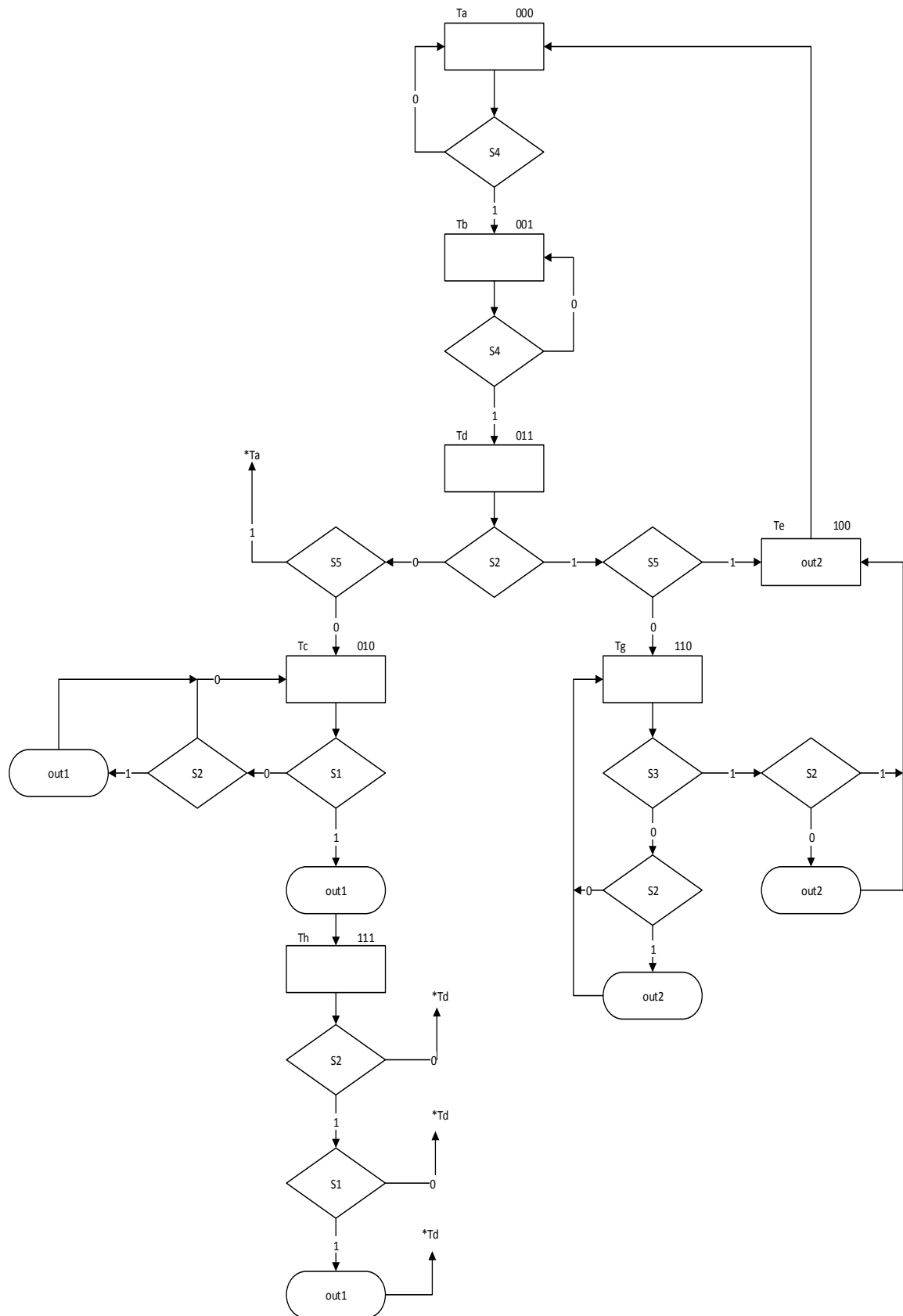
Problema # 2

Y2			Y1		
y_2/y_1	0	1	y_2/y_1	0	1
0	0	0	0	y_0S_4	0
1	$\overline{y_0}S_1 + y_0S_2$	$\overline{y_0}$	1	$\overline{y_0} + \overline{S_5}$	$\overline{S_3} + y_0$

y_2 / y_1	Y0	
	0	1
0	$y_0 + S_4$	0
1	$\overline{y_0}S_1$	y_0

y_2 / y_1	out1			
	00	01	11	10
0	0	$S_2 + S_1$	0	0
1	0	0	S_2S_1	0

y_2 / y_1	out2			
	00	01	11	10
0	0	0	$S_2 \oplus S_3$	1
1	0	0	0	0



```
library ieee;
use ieee.std_logic_1164.all;
```

```
entity Examen_1_2_2T is
port(Resetn, Clock: in std_logic;
S1, S2, S3, S4,S5: in std_logic;
Out1, Out2: out std_logic);
end Examen_1_2_2T;
```

architecture solucion of Examen_1_2_2T is

```
type estado is (Ta, Tb, Tc, Td, Te, Tg, Th);
```

```
signal y: estado;
```

```
begin
```

```
    process(Resetn, Clock)
```

```
    begin
```

```
        if (Resetn= '0') then y<=Ta;
```

```
        elsif (Clock'event and Clock= '1') then
```

```
            case y is
```

```
                when Ta =>
```

```
                    if S4='1' then y<=Tb;
```

```
                    else y<=Ta;
```

```
                    end if;
```

```
                when Tb =>
```

```
                    if S4='1' then y<=Td;
```

```
                    else y<=Tb;
```

```
                    end if;
```

```
                when Tc =>
```

```
                    if S1='1' then y<=Th;
```

```
                    else y<=Tc;
```

```
                    end if;
```

```
                when Td =>
```

```

        if S2='1' then
            if S5='1' then y<=Te;
            else y<=Tg;
            end if;
        elsif S5='1' then y<=Ta;
        else y<= Tc;
        end if;
    when Te =>
        y<= Ta;
    when Tg =>
        if S3='1' then y<=Te;
        else y<=Tg;
        end if;
    when Th =>
        y<=Td;
    end case;
end if;
end process;

```

--Salidas

```

process(y, S1, S2, S3, S4, S5)
begin
    case y is
        when Ta => out1<='0'; out2<='0';
        when Tb => out1<='0'; out2<='0';
        when Tc => out1<='0'; out2<='0';
        if S1='1' then out1<='1';
        elsif S2='1' then out1<='1';
        else out1<='0'; out2<='0';
        end if;
    end case;
end process;

```

```

when Td => out1<='0'; out2<='0';

when Te => out2<='1'; out1<='0';

when Tg => out1<='0'; out2<='0';

    if S3='1' then

        if S2='0' then out2<='1';

        end if;

    elsif S2='1' then out1<='1';

    else out1<='0'; out2<='0';

    end if;

when Th =>

    if (S2='1' and S1='1') then out1<='1';

    else out1<='0'; out2<='0';

    end if;

end case;

end process;

end solucion;

```

Problema # 3

